What is claimed is:

1. A synchronous memory device receiving a number of data synchronous with a rising edge and a falling edge of an operation clock, comprising:

data strobe buffering means for outputting a rising pulse and a falling pulse for detecting a rising edge and a falling edge of a DQS signal that sustains high impedance state when there is no operation and is clocked while the data is inputted;

data align latching means for latching and aligning the data synchronous with the rising pulse and the falling pulse; and

DQS signal controlling means for controlling the data strobe buffering means to output the rising pulse and the falling pulse to the data align latching unit only when the DQS signal is clocked.

2. The synchronous memory device as recited in claim 1, wherein the data strobe buffering means includes:

differential amplifying means for receiving the DQS signal and a reference voltage;

first buffering means enabled by a DQS pass signal that is outputted from the DQS signal controlling unit for buffering and outputting the output signal of the differential amplifying means;

second buffering means for buffering the output of the

first buffering means to output the rising pulse; and

third buffering means for buffering the output of the first buffering means to output the falling pulse.

3. The synchronous memory device as recited in claim 2, wherein the differential amplifying means includes:

a first and a second MOS transistors for receiving the reference voltage and the DQS signal at their gates, respectively;

a third diode-type MOS transistor coupled to a power voltage VDD and one end of the first MOS transistor, the gate of the third diode-type MOS transistor being coupled to the one end of the first MOS transistor;

a fourth MOS transistor coupled to the power voltage VDD and the one end of the second MOS transistor, the gate of the fourth MOS transistor being coupled to the gate of the third MOS transistor to form a current mirror; and

a fifth MOS transistor for connecting the commonly coupled other end of each of the first and the second MOS transistors to the ground voltage, and receiving, at its gate, the DQS enable signal that is generated by a write command.

4. The synchronous memory device as recited in claim 3, wherein the first buffering means includes:

a NAND gate for receiving the one end of the second MOS transistor and the DQS pass signal that is outputted from the

DQS signal controlling means; and

a first and a second inverters, serially coupled to each other, for buffering and outputting the output of the NAND gate.

5. The synchronous memory device as recited in claim 4, wherein the second buffering means includes:

a third inverter for outputting the inverted output of the second inverter; and

a fourth inverter for outputting the inverted output of the third inverter as the rising pulse.

6. The synchronous memory device as recited in claim 5, wherein the third buffering means includes:

a fifth inverter for outputting the inverted output of the second inverter;

a sixth inverter for outputting the inverted output of the fifth inverter; and

a seventh inverter for outputting the inverted output of the sixth inverter as the falling pulse.

7. The synchronous memory device as recited in claim 2, wherein the DQS signal controlling means includes:

DQS signal disabling means for outputting a DQS stop signal in the post-amble state of the DQS signal for stopping outputting of the DQS signal; and

DQS pass signal generating means for enabling the DQS

pass signal with a preamble pulse signal that is generated during the preamble period of the DQS signal, and disabling the DQS pass signal in response to the DQS stop signal.

8. The synchronous memory device as recited in claim 7, wherein the DQS pass signal generating means includes:

DQS state detecting means enabled by the DQS enable signal that is generated by the write command for changing the output to a first level in response to the preamble pulse signal that is generated in the preamble state of the DQS signal and changing the output to a second level in response to the DQS stop signal; and

DQS pass signal outputting means for latching and outputting the signal level of the output of the DQS state detecting means.

9. The synchronous memory device as recited in claim 8, wherein the DQS state detecting means includes:

a first MOS transistor receiving the DQS stop signal at its gate, one end of the first MOS transistor being coupled to the power voltage;

a second MOS transistor receiving the preamble pulse signal at its gate, one end of the second MOS transistor being coupled to the other end of the first MOS transistor;

a third MOS transistor receiving the preamble pulse signal at its gate, one end of the third MOS transistor being coupled to the other end of the second MOS transistor;

a fourth MOS transistor receiving the DQS enable signal at its gate, one end of the fourth MOS transistor being coupled to the other end of the third MOS transistor and the other end of the fourth MOS transistor being coupled to the ground voltage; and

a fifth MOS transistor receiving the DQS enable signal at its gate and connecting the power voltage to the common node of the second MOS transistor and the third MOS transistor.

10. The synchronous memory device as recited in claim 9, wherein the DQS pass signal outputting means includes:

a first inverter, its input being coupled to the power voltage and the common node of the second MOS transistor and the third MOS transistor;

a second inverter, its input and its output being coupled to the input and the output of the first inverter, respectively;

a third inverter for outputting the inverted output of the second inverter; and

a fourth inverter for outputting the inverted output of the third inverter as the DQS pass signal.

11. The synchronous memory device as recited in claim 7, wherein the DQS signal disabling means includes:

burst length detecting means for outputting a burst length signal that is enabled at the timing when the last data among a number of inputted data is inputted in a burst length

mode;

DQS pulse generating means for outputting a DQS pulse signal that is generated as a pulse at every timing when the DQS signal is clocked; and

DQS stop signal generating means for outputting the DQS stop signal by using the DQS pulse signal that is inputted while the burst length signal is enabled.

12. The synchronous memory device as recited in claim 11, wherein the DQS stop signal generating means includes:

a first NAND gate receiving the burst length signal and the DQS pulse signal;

a first NOR gate receiving the output of the first NAND gate and a DQS sustain signal that has the high level during an interrupt mode and a gapless mode; and

a first inverter for inverting the output of the first NOR gate to output the DQS stop signal.

13. The synchronous memory device as recited in claim 12, wherein the burst length detecting means includes:

a second NAND gate receiving a first burst length signal that sustains the enable state when the burst length mode is '4' and a first burst mode enable signal that is enabled at the timing when the fourth data is inputted during the period when the burst length mode is '4';

a third NAND gate receiving a second burst length signal that sustains the enable state when the burst length mode is

'8' and a second burst mode enable signal that is enabled at the timing when the eighth data is inputted during the period when the burst length mode is '8'; and

a fourth NAND gate receiving the outputs of the second NAND gate and the third NAND gate to output the burst length signal.

14. The synchronous memory device as recited in claim 13, wherein the DQS pulse generating means include:

a second inverter for outputting the inverted output of the first buffering means;

a third and a fourth inverter serially coupled to each other for buffering the output of the second inverter; and

a second NOR gate receiving the output of the first buffering means and the output of the fourth inverter to output the DQS pulse signal.

15. The synchronous memory device as recited in claim 1, wherein the DQS buffering means and the DQS signal controlling means are enabled by the DQS enable signal that is generated by a write command.